

The shifting paradigm of teaching and learning

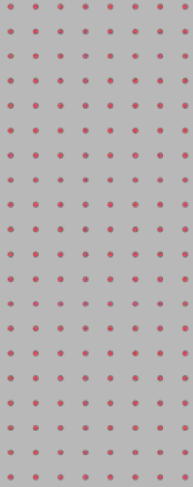
José Manuel Martins Ferreira | jmf@fe.up.pt | 26.01.2023

(online at <https://bit.ly/26-01-2023>)

Roadmap

1. Forces of change (power balance)
2. Personal experience
3. Conclusion

Forces of change (power balance)



Sort by Date ▾

→ Cinema
we are waching all your videos at the cinema today. Having discussions....

← @gmail.com
Re: Student survey
Is it ok if you get them on Thursday?
We worked from home and I don't h...

← @gmail.com
TO CCW3: Group 1 video
Hi, We ran into some problem with our video recording today, unfortun...

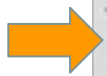
TO @gmail.com
Re: Student survey
I will do it tomorrow at school. Have a nice day! :) Sent from my iPhone

TO Video Presentation
Hello, Here comes the link to our last coursework video! BoundaryScanIn...

← @gmail.com
TO CCW3 video length
The video ended up being 13+ minutes long. Is this okay since the...

← @gmail.com
TO Re: Student survey
They are filled out, just waiting to meet Alex this week. Sent from my i...

Jose Manuel Martins Ferreira
TO DFDS-3101: Deliverables deadli...
Dear Class, Just a reminder that you're expected to submit your deli...



às 08:31
Inbox - HBV TW

To: Jose Ferreira
Cinema

we are waching all your videos at the cinema today. Having discussions. All the other rooms on campus are in use for exams.

Best regards

Assessment

- 50% of final grade comes from work at the end of the course (2 weeks out of 14 total)
- All assessment activities taking place during the course are collaborative (group graded, different grad in the same group are possible)
- The remaining 50% comes from the final exam (individual exam with no aids allowed)

jmf@fe.up.pt | <https://bit.ly/26-01-2023>

Education hashtag in Tiktok




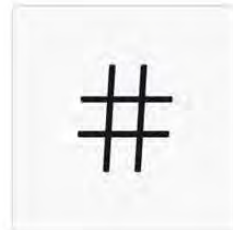
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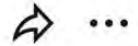
 Following

 LIVE

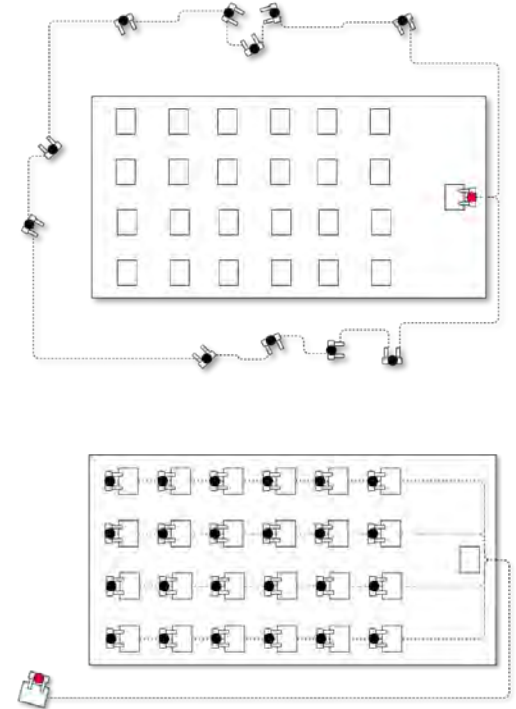
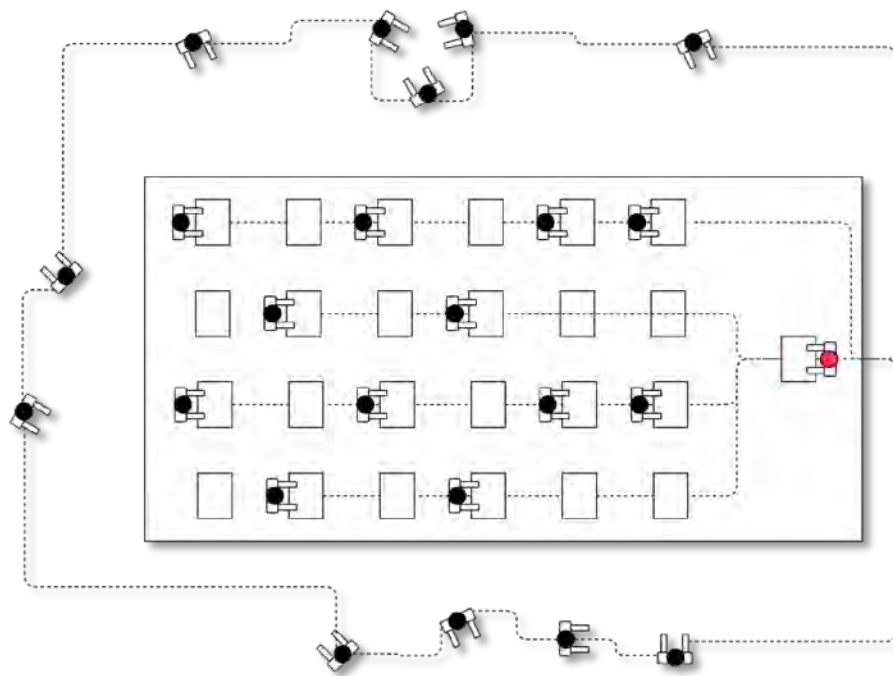


#education

45.7B views



“Tear down this wall!” (classroom)





“Tear down this wall!” (lab)

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Journal & Magazines > IEEE Transactions on Learning... > Volume: 2 Issue: 4

Remote Laboratories Extending Access to Science and Engineering Curricular

Publisher: IEEE [Cite This] [PDF]

Martyn Cooper; Jose M.M. Ferreira All Authors

68 Paper 1410 Citations Full Text Views

[Open Access]

Abstract

Abstract: This paper draws on research, development, and deployment of remote laboratories undertaken by the authors since 2000. They jointly worked on the PEARL project (<http://iet.open.ac.uk/pearl/>) from 2000 to 2005. They have worked on further projects within their own universities in the United Kingdom, and the University of Porto, Portugal.

More Like This

A visual electromagnetics laboratory for engineering education based on TLM Antennas and Propagation Society Symposium 1991 Digest Published: 1991

The use of computer-aided-instructions in computer engineering curriculum IEEE Proceedings of the SOUTHEASTCON '91 Published: 1991

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Conferences > 2014 11th International Confe...

Rise and fall of remote labs: Or perhaps not?

Publisher: IEEE [Cite This] [PDF]

José Manuel Martins Ferreira; Olaf Hallan Graven All Authors

94 Full Text Views

[R] [C] [Share] [Bell]

Abstract

Abstract: Offering Internet access to laboratory workbenches became trendy in the early years of the last decade [1,2]. Remote labs, in opposition to real labs, are frequently regarded as an extension of e-learning platforms, offering the advantages of online access to an area where educational practices remained largely unchanged since pre-e-learning times. This vision has frequently led many technology enthusiasts to jump ahead of pedagogical concerns, and explains why it is possible to find many remote labs that offer little or no added value to the teaching and learning process.

More Like This

Teaching Internet of Things in a Collaborative Laboratory Environment 2019 5th Experiment International Conference (exp at 19) Published: 2019

A system characterization/identification laboratory teaching tool for Internet 1996 IEEE International Conference on Acoustics, Speech, and Signal Processing Conference Proceedings Published: 1996

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Caitlin Cassidy Higher education reporter

Mon 16 Jan 2023 14:00 GMT



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Teachers are on alert for inevitable cheating after release of ChatGPT

ChatGPT offers a glimpse at a future in which computer-generated answers may be undetectable

By Laura Meckler and Pranshu Verma

December 26, 2022 at 6:00 a.m. EST



ChatGPT

JO tell me about life on Mars



Life on Mars is currently not known to exist. However, scientists believe that microbial life may have existed on Mars in the past and continue to study the planet in the hopes of finding evidence of past or present life. NASA and other space agencies have sent missions to Mars to study its geology, atmosphere, and potential for human habitation in the future. As of 2021, NASA's Perseverance rover has successfully landed on Mars and is currently exploring Jezero crater to study the past habitability of Mars.

JO but were there humans on Mars before?



No, there have not been any humans on Mars. Currently, there are no manned missions to Mars, and it is not yet known when or if humans will ever be able to travel to and live on Mars permanently. The technology and resources required for human travel to and habitation on Mars are still being developed and tested. NASA's Artemis program aims to land the first woman and next man on the Moon by 2024 and eventually establish a sustainable presence on the Moon, which will serve as a stepping stone for future human missions to Mars.

JO please don't be so verbose



Humans have not been to Mars. NASA plans to land astronauts on the Moon by 2024 as a step towards sending humans to Mars.

JO Do you know what is a sensitivity list in VHDL?



In VHDL, a sensitivity list is a list of signals that a process is sensitive to. A process is a concurrent statement that describes the behavior of a digital system. It is executed in parallel with other processes. A process waits for changes on the signals in its sensitivity list, and when a change occurs on one of the signals, the process is activated and its statements are executed. The sensitivity list is specified in the "wait on" clause of the process statement.

For example, if a process is sensitive to changes on signals A and B, the sensitivity list would be specified as:

```
process(A, B)
begin
  -- process statements
end process;
```

Copy code

The process will be activated every time there's a change on either A or B. If the sensitivity list is omitted, the process will not be activated by any signal, so it will have to wait for an explicit "wait" statement.

ChatGPT

Jo what is the syntax of the when/else statement in VHDL? ←

In VHDL, the "when/else" statement is used to provide a conditional branch in a process or an architecture. The "when" part of the statement specifies the condition, and the "else" part of the statement specifies the action to be taken if the condition is not met.

The general syntax of a "when/else" statement in VHDL is as follows:

```
when <condition> =>
  <statement1>;
  <statement2>;
  ...
else
  <statement3>;
  <statement4>;
  ...
end when;
```

Where:

- * <condition> is an expression that evaluates to true or false.
- * <statement1>, <statement2>, ... are the statements that are executed when the condition is true.
- * <statement3>, <statement4>, ... are the statements that are executed when the condition is not true.

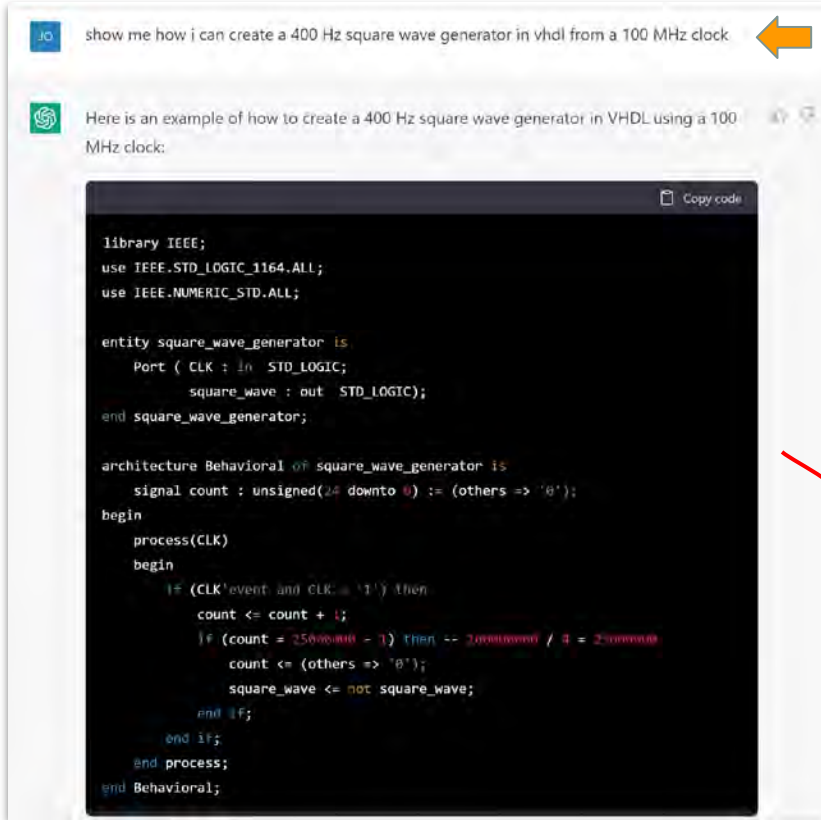
The "when/else" statement can be used inside a process or an architecture, and it can be nested within other "when/else" statements. It's important to note that only one branch of a when/else statement will be executed based on the condition.

Here's an example of a when/else statement in VHDL:

```
process(clk)
begin
  if rising_edge(clk) then
    if reset = '1' then
      count <= (others => '0');
    else
      when count < max_count =>
        count <= count + 1;
      else
        count <= (others => '0');
      end when;
    end if;
  end if;
end process;
```

In this example the process is sensitive to the clock edge, if the edge is rising and the reset signal is '1' then the count variable is set to zero, otherwise, if the count is less than max_count, it will increase by 1, otherwise, it will be set to zero.

ChatGPT



JO show me how i can create a 400 Hz square wave generator in vhdl from a 100 MHz clock

Here is an example of how to create a 400 Hz square wave generator in VHDL using a 100 MHz clock:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity square_wave_generator is
  Port ( CLK : in STD_LOGIC;
        square_wave : out STD_LOGIC);
end square_wave_generator;

architecture Behavioral of square_wave_generator is
  signal count : unsigned(24 downto 0) := (others => '0');
begin
  process(CLK)
  begin
    if (CLK'event and CLK = '1') then
      count <= count + 1;
      if (count = 25000000 - 1) then -- 100000000 / 4 = 25000000
        count <= (others => '0');
        square_wave <= not square_wave;
      end if;
    end if;
  end process;
end Behavioral;
```

This VHDL code uses a 100 MHz clock as an input and generates a 400 Hz square wave as an output. The square wave frequency is determined by the value assigned to the "count" signal in the "if (count = 25000000 - 1)" statement. In this case, 25000000 is calculated by dividing the clock frequency (100 MHz) by the desired frequency of the square wave (400 Hz) times 2 (for a square wave). The output square_wave is toggled everytime the count reaches the value of 25000000-1.

ChatGPT

JO write a 100-word on cryptography in the style of isaac asimov



Cryptography, the art and science of securing communication, has always been an essential tool for humanity. From the ancient Egyptians who used hieroglyphs to hide messages, to the modern computer algorithms that protect our online transactions, cryptography has enabled us to share information safely. As technology advances and new forms of communication emerge, the need for cryptography becomes even more vital. However, it is not only a tool for secrecy, but also for authenticity, integrity and non-repudiation. With the advent of Quantum Computing, the future of cryptography is uncertain but what is certain is that the quest for secure communication will continue. The need for secrecy is as old as human civilization itself and will be with us as long as we need to communicate.

JO rephrase in the style of james joyce



Cryptography, that obscure and abstruse art of communication security, has ever been a vital instrument for mankind. From the hieroglyphs of ancient Egypt, which concealed messages, to the algorithmic intricacies that safeguard our digital transactions, the need for cryptography is a ceaseless one. As technology progresses and new forms of communication arise, the requirement for cryptography becomes all the more imperative. But it is not solely a tool for secrecy, but also for authenticity, integrity and non-repudiation. The future of cryptography is uncertain with the advent of Quantum Computing, but the need for secure communication remains constant, as ancient as human civilization itself and will persist as long as the need to convey endures.

JO make it shorter and translate to Norwegian

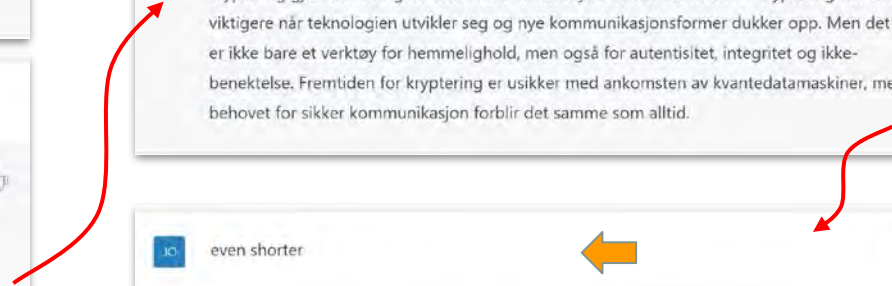


Kryptering, kunsten og vitenskapen om å sikre kommunikasjon, har alltid vært et viktig verktøy for menneskeheten. Fra det gamle Egypt som brukte hieroglyfer for å skjule meldinger, til moderne datamaskin algoritmer som beskytter våre online transaksjoner, har kryptering gjort det mulig for oss å dele informasjon sikkert. Behovet for kryptering blir enda viktigere når teknologien utvikler seg og nye kommunikasjonsformer dukker opp. Men det er ikke bare et verktøy for hemmelighet, men også for autentisitet, integritet og ikke-benektelse. Fremtiden for kryptering er usikker med ankomsten av kvantedatamaskiner, men behovet for sikker kommunikasjon forblir det samme som alltid.

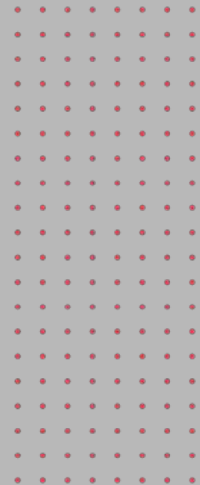
JO even shorter



Kryptering sikrer kommunikasjon og har alltid vært viktig for menneskeheten. Fra gamle hieroglyfer til moderne algoritmer, har kryptering gjort det mulig å dele informasjon trygt. Behovet for kryptering øker med teknologisk utvikling, men ikke bare for hemmelighet, men også for autentisitet, integritet og ikke-benektelse. Fremtiden for kryptering er usikker med kvantedatamaskiner, men behovet for sikker kommunikasjon forblir det samme.



Personal experience



The course facilitator role

TSD3070: Digital Circuit Synthesis (2022/23)			
WEEK 0 (Prior reading)	Main topic & complementary information	Canvas content	
(self-study)	Setup and acquaintance - Basys-3 master constraints file	VIDEO: Welcome to this course! TOOL & LAB: Installation of Xilinx Vivado VIDEOS & LAB: Lab setup and acquaintance DISCUSSION: Concurrent nature of VHDL	
LECTURES' WEEK	Main topic & complementary information	Canvas content	Lectures (7 lectures per day from 9 am to 4:15 pm)
Monday 09.01 (K_2229) 09:00-09:45 11:00-11:45 12:30-13:15 15:30-16:15	VHDL/FPGA recap - code folder link - templates for a FSM and a FSM testbench - Pong Chu's book	VIDEOS & LABS: VHDL and FPGAs intro VIDEOS & LABS: Combinational circuit design VIDEOS & LAB: Regular sequential circuits VIDEOS & LAB: Finite state machines LAB: An FSM-based cheating e-dice DISCUSSION: Sensitivity list	1. Introduction and practical arrangements 2. The VHDL design file (e.g., multiply by adding: top level & ctr path) 3. Regular sequential circuits and finite state machines 4. E-dice: introduction, block diagram, creating the output table 5. E-dice: Vivado project, experimentation 6. E-dice cheating plus version: presentation and experimentation 7. Sensitivity list discussion, plan for tomorrow
Tuesday 10.01 (K_2229) 09:00-09:45 11:00-11:45 12:30-13:15 15:30-16:15	The IEEE 1149.1 BST embedded test logic - course folder link	VIDEOS: Introduction to the BST std LAB: Operation of the embedded test logic DISCUSSION: The test cells DISCUSSION: The BS instruction register DISCUSSION: Timing issues: Delay between TAP states	1. Introduction to BST (why, overview of test logic and fault detection) 2. The BS cell (operation and VHDL description), the embedded test logic 3. IR and BP cells (operation and VHDL descriptions), the BST instructions 4. The TAP controller: operation and VHDL description 5. Trainer 1149.1 : Hands-on BS chain operation 6. Putting it all together, SN74BCT8244 data sheet revisited 7. Timing issues discussion, plan for tomorrow
Wednesday 11.01 (K_2229) 09:00-09:45 11:00-11:45 12:30-13:15 15:30-16:15	BST board testing - notes folder link	VIDEOS: Fault detection with BST DISCUSSION: SN74BCT8244: Output pin control DISCUSSION: SN74BCT8244: Output behaviour DISCUSSION: Open fault inside a cluster	1. Recap of yesterday 2. Board testing (BS chain, shorts and opens) 3. Board test: short-circuit among pins in different chains (X9) 4. Board test: open-circuit fault inside cluster (X1) 5. Board test: short-circuit fault inside cluster (X2) 6. Board test: infrastructure fault (X16) 7. SN74BCT8244 PRPG and SA modes, plan for tomorrow
Thursday 12.01 (K_2229) 09:00-09:45 11:00-11:45 12:30-13:15 15:30-16:15	Finite State Machines with Datapath (introduction) - code folder link - templates for top level and an RS232 testbench	VIDEOS & LAB: Finite state machines with datapath LAB: Receive ASCII via RS232 and display on Basys-3	1. Introduction to FSMs (what, ASMD representation rules) 2. Multiply by adding: FSM architecture and operation 3. Multiply by adding: ASMD chart 4. Multiply by adding: Vivado project 5. Multiply by adding: Vivado project and experimentation 6. Multiply by adding: single file implementation 7. Display ASCII codes received via RS232 (lab script), plan for tomorrow
Friday 13.01 (K_2229) 09:00-09:45 11:00-11:45 12:30-13:15 15:30-16:15	Finite State Machines with Datapath (practice) - code folder link	VIDEO & LAB: Napoleon's cipher DISCUSSION: Napoleon's cipher handling backspaces	1. Introduction to Napoleon's cipher (operation) 2. Napoleon's cipher: FSM architecture 3. Napoleon's cipher: ASMD chart 4. Napoleon's cipher: Vivado project 5. Napoleon's cipher: Vivado project and experimentation 6. Introduction to the first coursework assignment (with demo) 7. Wrap-up and plan for the following weeks

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2023 VAR

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Published Edit

W1D1: VHDL and FPGAs intro (videos & labs)

02a Groundwork statements

- VHDL is a **concurrent language by nature** (because it is a *HDL*...)
- “Concurrent statements execute asynchronously with respect to each other” (IEEE 8008, p. 169)

```

Port ( in1, in0, en: in STD_LOGIC;
      out3, out2, out1, out0: out STD_LOGIC
);
architecture darch of dec2to4 is
begin
  out3 <=
  out2 <=
  out1 <=
  out0 <=
end darch;

```

What does VHDL mean?

These statements execute in parallel

Watch on YouTube

N.B.: The playlist above comprises five presentations.

Learning outcomes (you'll be able to...):

- Explain the basic rules governing the use of VHDL
- Distinguish between concurrent and sequential statements
- Explain the differences between dataflow, behavioral and structural modelling styles (architecture section)
- Explain what is type casting and why it is necessary

2023 VAR

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W7-W9: FSM design (discussion)

Jose Ferreira

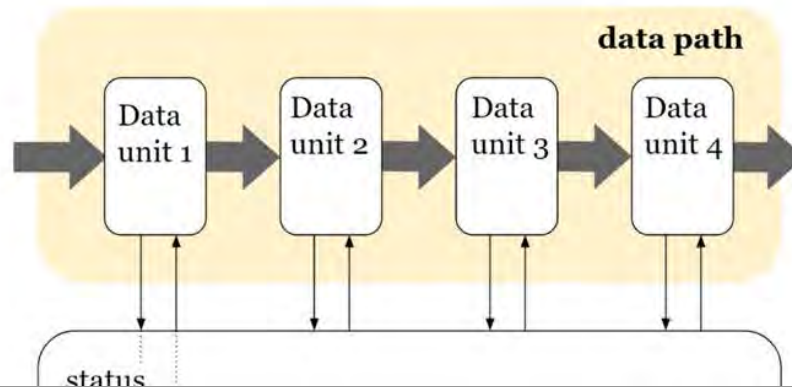
All sections

13 Dec 2022 at 11:29

These questions are presented under the following assumptions:

- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

Consider the following general representation of a Finite State Machine with Datapath (FSMD) architecture.







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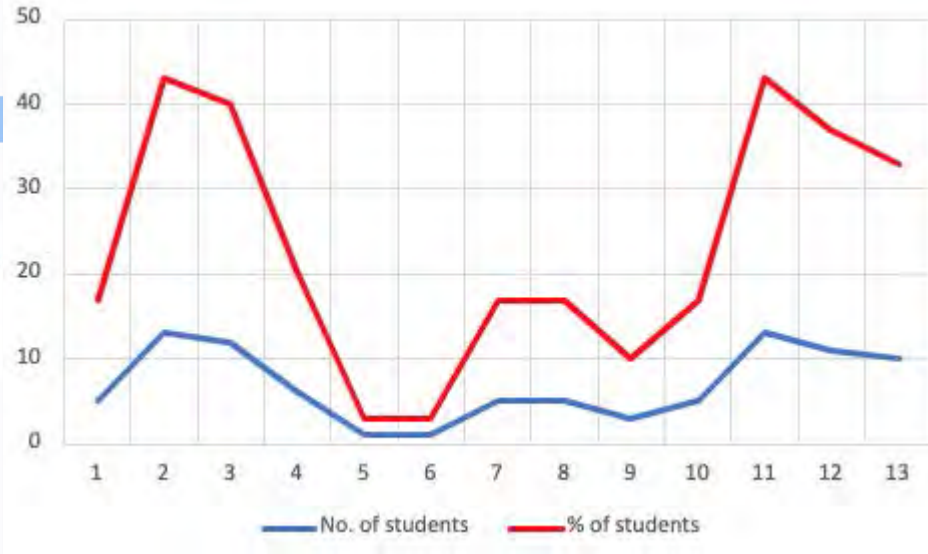
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“Tear down this wall!” (classroom)

From 12/01/2021 to 12/01/2021

Maximum report duration: 1 Month

Reports show information for meetings that ended at least 15 minutes ago.



Meeting ID	Start Time	End Time	Duration (Minutes)	Participants	Source
CS4110: Day start-up meet...	7355	9010	1655	3	LTI Pro
CS4110: Day start-up meet...	9107	2988	1977	8	LTI Pro
CS4110: Day start-up meet...	9107	2988	1977	6	LTI Pro
CS4110: Day start-up meet...	9107	2988	1977	16	LTI Pro
CS4110: Day start-up meet...	9107	2988	1977	14	LTI Pro
CS4110: Day start-up meet...	9107	2988	1977	7	LTI Pro
CS4110: Day start-up meet...	9107	2988	1977	7	LTI Pro

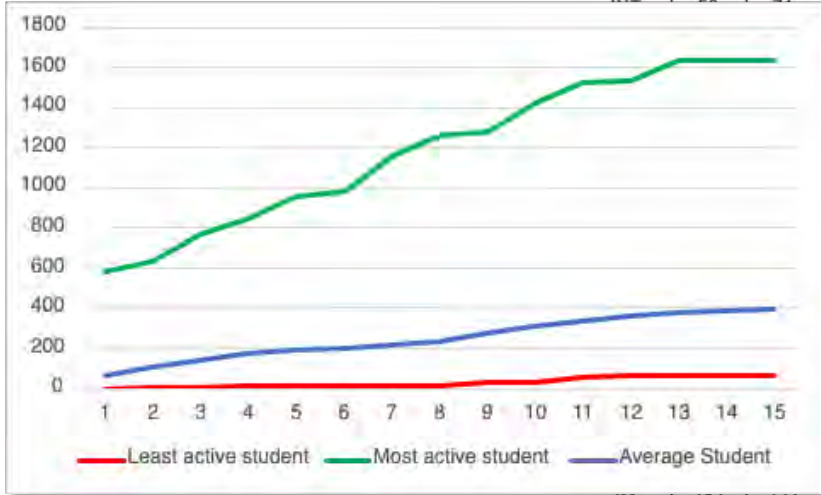
Group	Has Zoom Rooms?	Creation Time	Start Time	End Time	Duration (Minutes)	Participants	Source
	No	10/27/2021 12:19:51 PM	11/08/2021 08:20:33 AM	11/08/2021 08:32:14 AM	12	3	LTI Pro
	No	10/27/2021 12:19:51 PM	11/08/2021 08:32:19 AM	11/08/2021 09:57:11 AM	85	8	LTI Pro
	No	10/27/2021 12:50:04 PM	11/09/2021 08:15:08 AM	11/09/2021 09:25:39 AM	71	6	LTI Pro
	No	10/27/2021 12:51:18 PM	11/10/2021 08:12:59 AM	11/10/2021 09:29:15 AM	77	16	LTI Pro
	No	10/27/2021 12:55:00 PM	11/11/2021 08:11:21 AM	11/11/2021 09:29:11 AM	78	14	LTI Pro
	No	10/27/2021 12:57:04 PM	11/12/2021 08:16:54 AM	11/12/2021 09:13:09 AM	57	7	LTI Pro
	No	10/27/2021 12:57:04 PM	11/12/2021 08:16:54 AM	11/12/2021 09:13:09 AM	57	7	LTI Pro
	No	10/27/2021 12:57:04 PM	11/12/2021 08:16:54 AM	11/12/2021 09:13:09 AM	57	7	LTI Pro

Jose Ferreira Jose.Ferreira@usn.no
 Jose Ferreira jmf@fe.up.pt | https://bit.ly/26-01-2023



“Tear down this wall!” (classroom)

Student	< 8.11	8.11	9.11	10.11	11.11	12.11	13.11	14.11	15.11	16.11	17.11	18.11	19.11	20.11	21.11
INT	1	9	15	26	33	35	35	35	67	94	129	147	147	147	149
INT	7	18	46	79	84	84	84	116	136	140	145	147	164	164	164
FT	1	78	95	148	203	268	316	336	357	366	376	381	383	383	383
INT	52	72	74	74	141	141	141	285	295	305	341	341	348	374	374
INT	132	169	193	203	203	203	215	363	473	483	507	516	516	537	537
INT	218	267	343	354	354	354	398	429	526	567	627	636	636	636	636
INT	8	10	14	16	16	16	16	27	27	56	62	64	64	64	64
INT	92	92	92	95	95	95	95	115	127	152	152	155	155	155	155
INT	172	172	172	172	228	263	263	541	646	832	952	983	1064	1178	1178
INT	105	111	131	135	164	168	168	200	213	219	228	236	236	288	288
INT	22	24	24	24	24	24	26	43	73	79	86	86	86	103	103
INT	40	44	50	50	50	50	50	83	106	106	125	132	132	132	132
INT	771	849	960	978	1156	1258	1258	1280	1422	1523	1532	1635	1635	1635	1635
INT	215	307	325	326	335	336	336	433	452	483	498	538	538	542	542
INT	10	12	16	18	18	18	18	32	48	58	74	86	86	86	86
INT	200	212	221	224	227	238	238	252	259	272	282	291	297	300	300
INT	25	50	60	64	64	64	64	81	102	118	133	159	159	159	159
INT	70	70	70	70	70	70	70	84	87	92	100	115	115	155	155
INT	180	234	259	263	267	290	290	298	364	375	428	430	430	430	430
INT	183	183	183	183	191	211	211	212	231	252	253	261	264	269	269
IM	134	141	155	197	202	202	204	208	214	214	214	217	225	226	226
INT	94	167	232	280	301	363	363	363	398	411	448	459	472	477	489
FT	35	80	131	160	184	184	200	237	255	261	273	297	300	300	305
IM	0	15	57	62	73	79	79	79	97	98	103	108	112	116	116
INT	144	181	284	409	416	416	416	416	558	674	796	900	1011	1011	1011
INT	79	214	243	243	286	308	324	324	365	469	520	566	577	577	577



Video content for course delivery

Video analytics

Overview Reach Engagement Audience

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+ "Average view duration
/ percentage viewed")

Key moments for audience retention

Average view duration

2:34

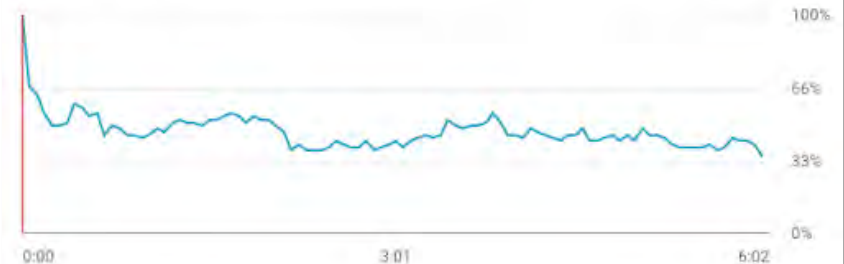
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42.7%



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An Innovative Course Delivery Model for Industry-Master Programs – Presentation of a Case-Study at the University of South-Eastern Norway

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Manuel Martins Ferreira All Authors

Document Sections

- i. Introduction
- ii. The Industry-Master Concept
- iii. The Cs Delivery Model
- iv. The Importance of

Abstract: This paper presents the teaching and learning model adopted in an industry-supported master program in Computer Science (MACS/MACSI) and discusses the importance of learning analytics to cope with the challenges posed by a delivery model where the courses run serially over 6 weeks (instead of running in parallel). This model was well received by the students, but calls for innovative pedagogical methods, where flexibility is particularly important for those students that are working in the partner companies. The long-term goal is to offer the same teaching and learning experience to both students and teachers, regardless of their location (on-campus or online), while offering an educational experience that is relevant both for the students and for their industry employers.

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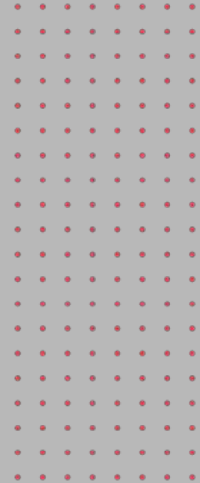
ChatGPT as a teaching assistant

Recommendation to students

VHDL and ChatGPT

- ChatGPT is a great source of help to clarify doubts
- Possibly the most important aspect (as in many other situations in life...) is to know what questions to ask
- Create an account at <https://chat.openai.com/> and avoid peak times

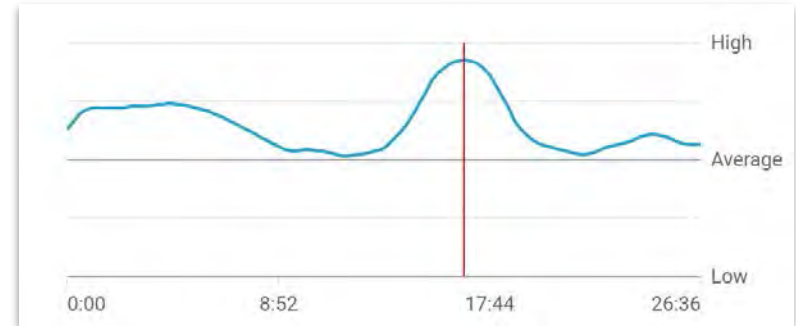
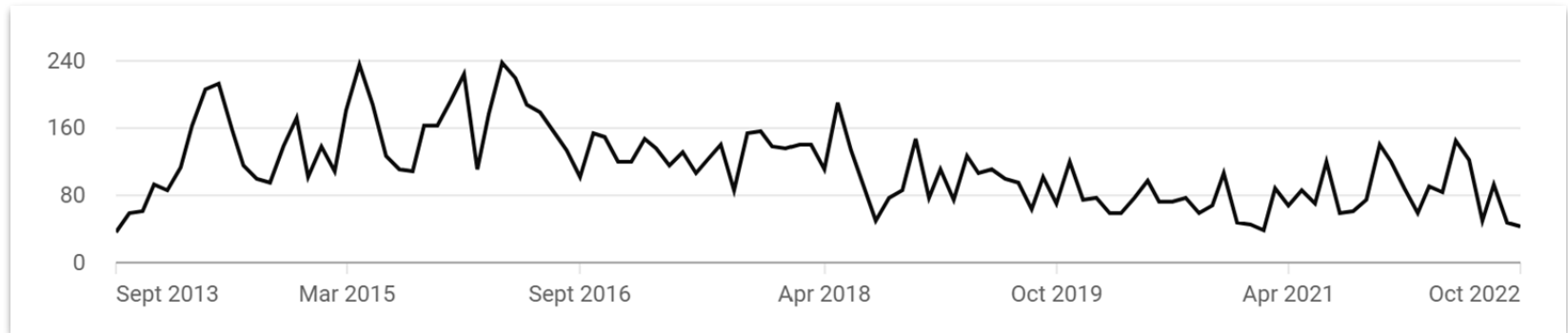
Conclusion



Challenges vs. opportunities

- “Course facilitator” profile:
 - Provide organization and context (what, when, who, how)
 - Adapt existing materials to new T&L contexts (e.g., transform slide sets into short video presentations)
 - Integrate new tools as they emerge (e.g., ChatGPT)
 - Always innovate (what comes next?)

Learn from bad/poor videos



Video transformation

SEGMENT 2 OF 4

Transcript Summary

02d Groundwork

Common concurrent statements

- The most common concurrent statements are:
 - Concurrent signal assignment
 - Conditional signal assignments
 - Selected signal assignments
 - Process statement (used to encapsulate sequential statements)

(check IEEE-2008 / chapter 11 for further details)

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There are four main concurrent statements that we will use extensively during this course: concurrent signal assignments, conditional and selected signal assignments, and the process statement that encapsulates the execution of sequential statements. Chapter 11 of the IEEE-2008 standard provides further details and describes additional concurrent statements, but for now it is sufficient to know those that will be presented here. Concurrent signal assignments are the type of statements that we have seen before in the dataflow description of the 2 to 4 decoder. They will become sequential signal assignments when encapsulated inside a process, but when used as shown here, they will be executed concurrently and therefore are concurrent signal assignments.

Sensitivity list

- The process is activated whenever at least one signal in its sensitivity list changes its value
- Choosing the signals to include in the sensitivity list is critical (and a frequent source of design problems)
- A process without a sensitivity list will trigger immediately

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statement
concurrent
signal assignments
process
sequential
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(R)labs for formative assessment



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Embedding formative assessment features into LabView interfaces

Embedding formative assessment features into LabView interfaces

Max Conradi¹, Reinhard Langmann¹, António M. Cardoso², J. M. Ferreira²
¹ University of Applied Sciences, Dusseldorf, Germany
² Faculdade de Engenharia, Universidade do Porto, Portugal

Abstract— Virtual instruments (VI), namely those designed using LabView, are increasingly used to enable access to remote instruments over the web. In an academic context, such VIs may be used to build a remote workbench that enables the students to carry out a laboratory task from their homes. Remote workbenches, or simulation environments, are not meant to replace real labs, but rather to complement them. They enable the students to continue their work in the lab, even after leaving the university campus. In most cases, a remote workbench constitutes a replica of what the student sees in a real workbench. However, VI interfaces may be designed to provide a much richer educational experience, namely by embedding formative assessment features, as described in this work-in-progress paper.

Index Terms— e-learning, formative assessment, online labs, LabView. jmf@fe.up.pt | <https://bit.ly/26-01-2023>

II. REFERENCE MODEL

The PTSE lab at FEUP already uses various VIs that are used to design remote experiments in electronics. All such VIs were developed using LabView. The proposed approach consists of analysing the LabView scripts for such VIs and devising ways to identify and capture the relevant embedded assessment information. In the initial phase of this work, a simple VI representing a basic instrument (e.g. a voltmeter) was used to look for an

Let ChatGPT have a say :)



what do you think about remote labs?



As a machine learning model, I do not have personal opinions or feelings. However, I can provide information on the topic of remote labs.

Remote labs, also known as virtual labs or online labs, are laboratory environments that are accessed remotely, typically through the internet. They allow students and researchers to access laboratory equipment, simulations, and other resources from anywhere, at any time.

Remote labs have a number of advantages over traditional, physical labs. They can provide access to equipment and resources that might not be available locally, and they can also allow for more flexible scheduling and greater collaboration among students and researchers. Additionally, remote labs can also be used to increase the number of students that can access equipment and resources, and they can also be used to provide access to labs for remote students or students in different locations.

However, remote labs also have some limitations. They may not be able to replicate all of the features and capabilities of physical labs, and they may also require specialized equipment or software to access. Additionally, they also might require internet access and a reliable connection, which can be an issue in some locations.

Overall, remote labs can be a valuable tool for students and researchers to access laboratory equipment and resources, but the limitations should be taken into account when planning and using them.



will remote labs replace real labs?



It is unlikely that remote labs will completely replace traditional, physical labs. While remote labs have a number of advantages, such as greater flexibility and accessibility, they also have limitations that may make them less suitable for certain types of experimentation or research.

Physical labs provide hands-on experience and the ability to work with real equipment and materials, which can be difficult to replicate in a remote environment. Additionally, remote labs may not be able to replicate all of the features and capabilities of physical labs, and they may also require specialized equipment or software to access.

Moreover, some experiments and research require the use of hazardous or toxic materials that are not suitable to be used in a remote environment and can only be used in physical labs.

However, remote labs can be a valuable supplement to traditional, physical labs, by allowing students and researchers to access equipment and resources that might not be available locally, and by providing a more flexible and collaborative environment for experimentation and research. Remote labs can also be useful for providing additional access to labs for remote students or students in different locations, or increasing the number of students that can access equipment and resources.

In conclusion, remote labs can be a powerful tool for conducting research and experiments, but it's unlikely that they will completely replace traditional physical labs, as both have their unique advantages and disadvantages that make them suitable for different types of research and experiments.

Let you have a say now! :)

José Manuel Martins Ferreira | jmf@fe.up.pt | 26.01.2023

(online at <https://bit.ly/26-01-2023>)

