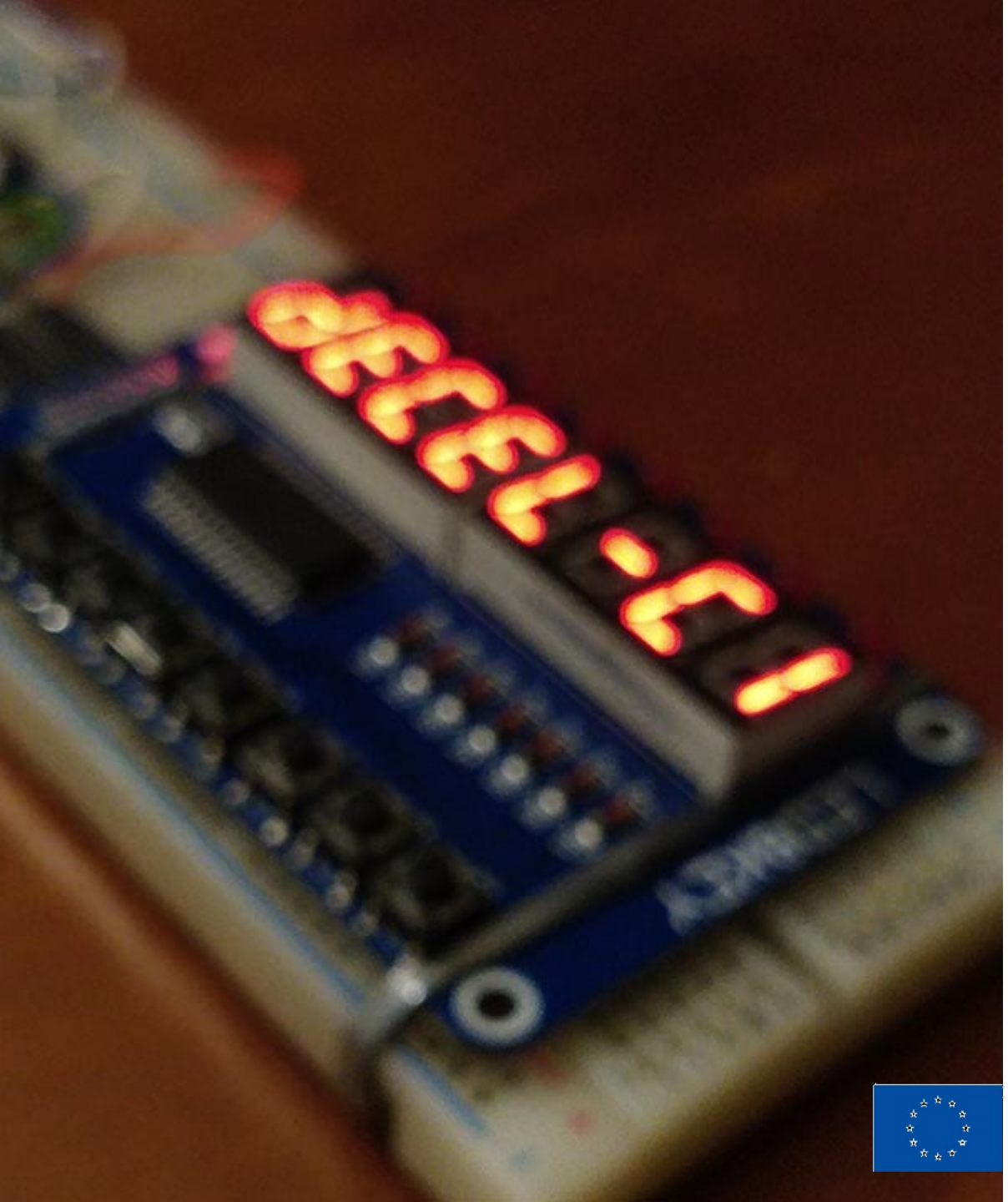


DECEL

Training activity C1

Applying novel pedagogical methods and tools to the teaching activity for Digital Electronics Systems

Porto, 25-27 January 2023

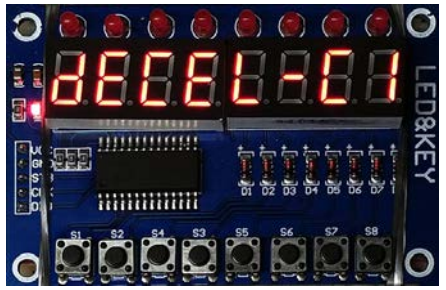
Co-funded by the European Union

Universidade do Porto

Faculdade de Engenharia

FEUP

Digital systems design at UP



- Digital systems
  - Introductory course on digital systems (logic level, introduction to uP organizatrion)
  - BSc, 1st year, 52h of classes, 162h of work, 300 students
- Digital Systems Design
  - Digital design for integrated technologies (RTL/logic level, Verilog, synthesis for FPGA)
  - MSc, 1st year, 39h of classes, 162h of work, 50 students
- VLSI Circuit design
  - Physical design for interated technologies (CMOS, transistor level, manual layout design)
  - MSc, 1st year, 39h of classes, 162h of work, 20 students
- Heterogeneous Systems Architectures
  - From software to sw+hw systems (CPU+FPGA, high-level synthesis, optim. for performance)
  - MSc, 2nd year, 39h of classes, 162h of work, 8 students

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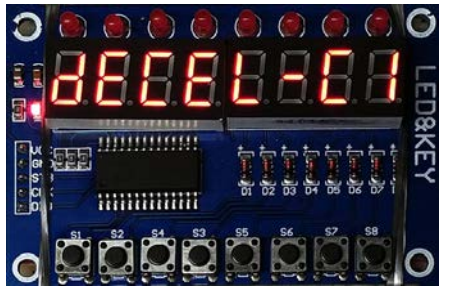
Common to all courses



- Strong laboratory work component
  - Building and experimentation of digital systems, for the introductory course
  - Practicing with EDA industrial tools, using whenever possible free EDA tools
- HDL used is Verilog, not VHDL
  - Light introduction in the first course
  - Main tool in the advanced digital design course, marginal use in the others
- EDA industrial tools provided by Europractice
  - XILINX ISE/Vivado/Vitis, Cadence, Synopsys, Siemens
- Moodle: sharing docs, evaluation, submission of written works
- No remote labs, mixed traditional teaching and project-based

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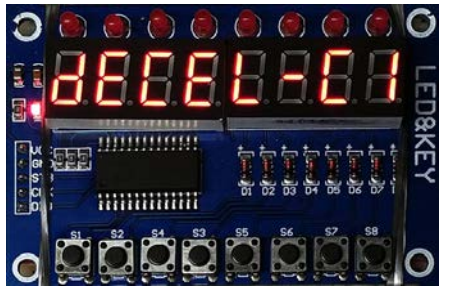
Digital systems (intro)



- To be presented by Hélio Mendonça

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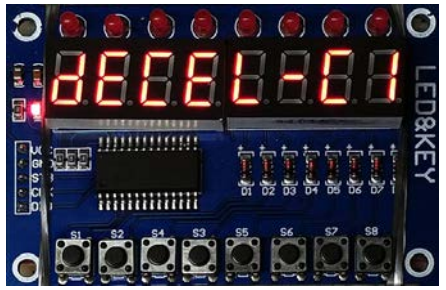
Digital Systems Design
(from HDL models to logic gates)



- Coding in Verilog HDL for RTL synthesis
- Functional verification with logic simulation, construction of testbenches
- RTL synthesis and logic optimization, IP integration
- Understanding the backend design stages, physical synthesis (P&R)
- Timing issues of clocked synchronous systems
- RTL design optimization for speed and area, speed/area tradeoffs
- Architectures for custom arithmetic operators
- The CORDIC algorithm and implementations

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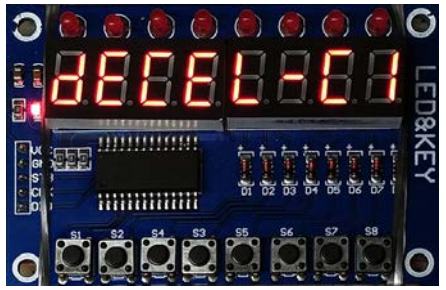
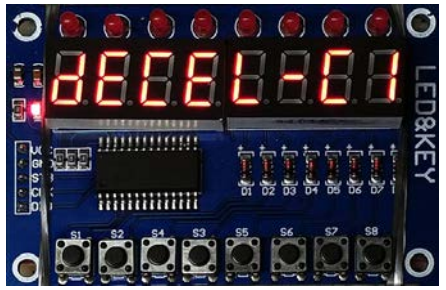
Digital Systems Design
(from HDL models to logic gates)

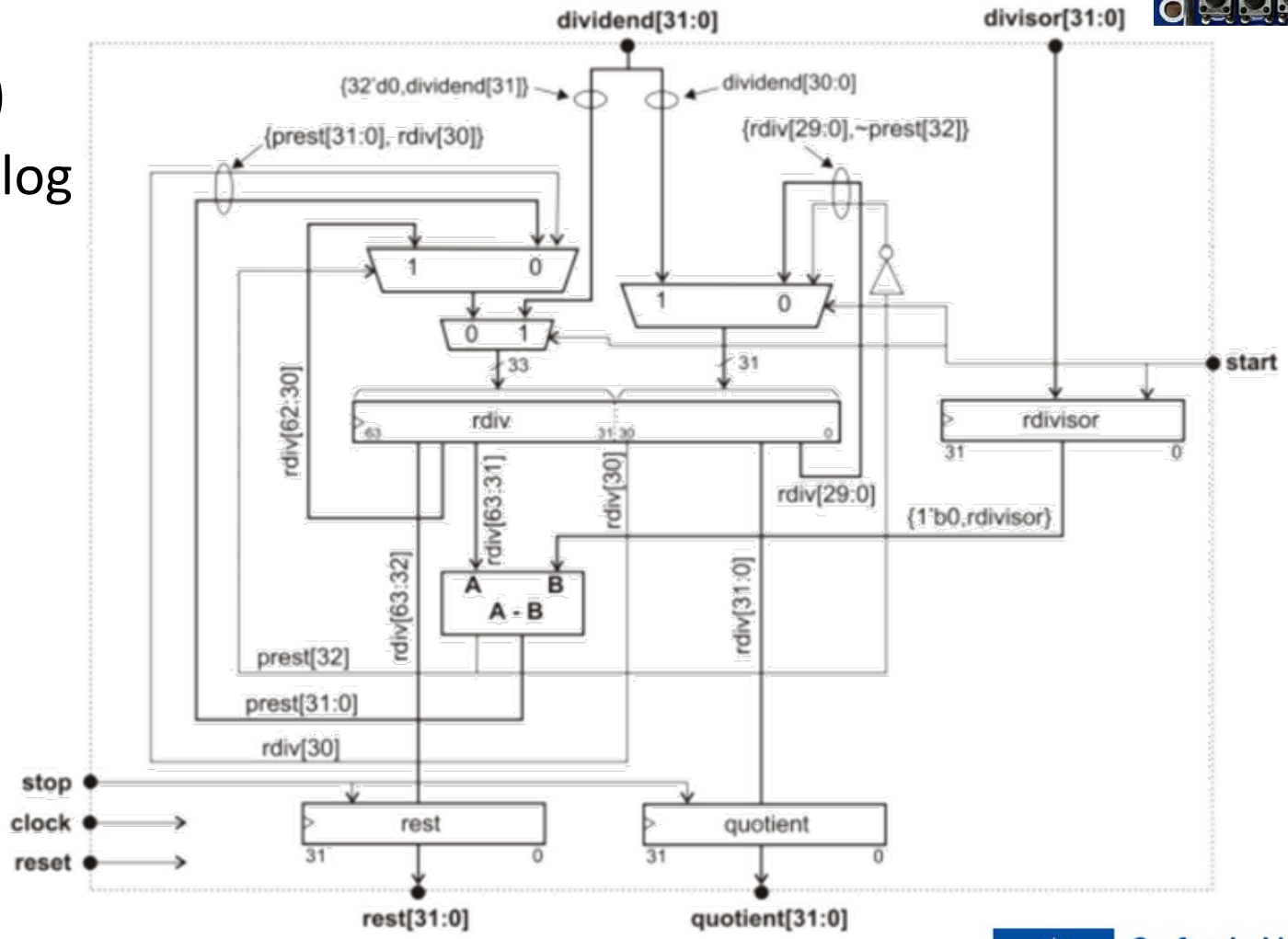


- Lectures (1.5h / week)
  - Traditional lectures, based on slides, white board, sharing experiences
- Lab classes (1.5h/week)
  - Guided tutorials to learn the EDA tools and to apply the design concepts
  - Logic simulation, coding in Verilog, RTL synthesis and physical implementation
  - Presentation, discussion and accompaniment of the 3 grading assignments
- Laboratory assignments
  - Groups of two students (not enough resources for individual works)
  - EDA tools used: QuestaSim (Siemens), XILINX ISE, Icarus Verilog/GTKWavem (free)

Digital Systems Design
(from HDL models to logic gates)



- Project 1 (10%)
  - Coding in Verilog



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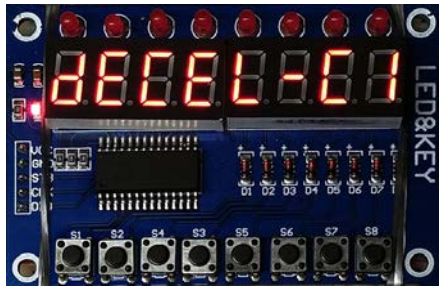
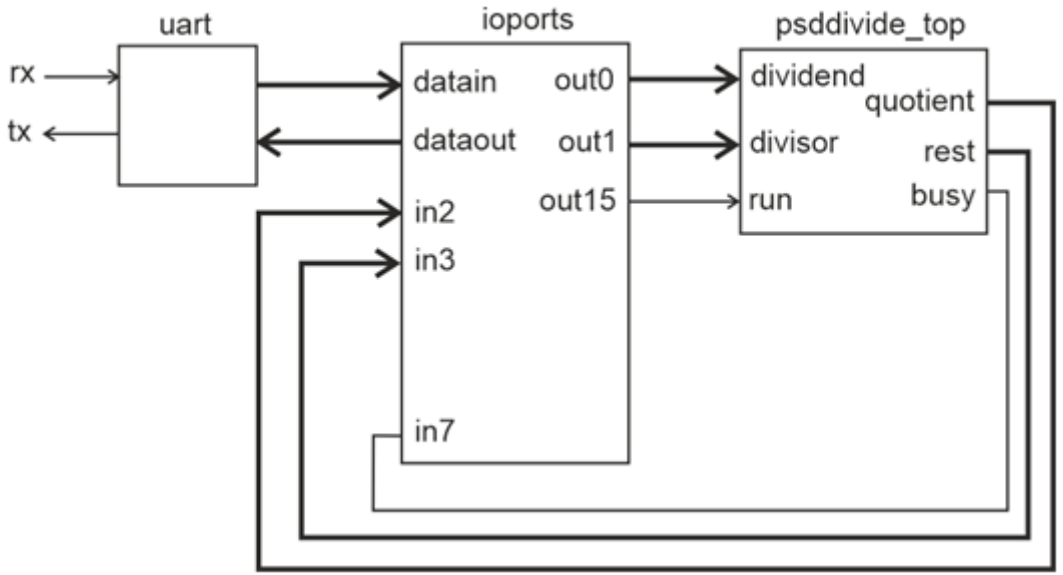
Digital Systems Design
(from HDL models to logic gates)



- Project 2 (5%)
  - Guided tour of XILINX ISE
  - RTL code is given
  - Physical experimentation



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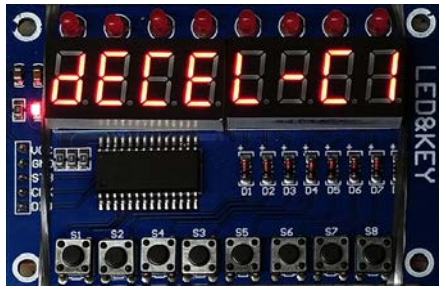
Digital Systems Design
(from HDL models to logic gates)



- Project 3 (35%)
  - Final integration project, addressing most of the design topics studied
  - Minimum 5 weeks allocated, groups of two students, some work alone
  - Specification of the system and the lab guide is constructed iteratively
  - Realistic system, final objective is to build the circuit in the FPGA board
  - The students need to develop only a “small” part of the system
  - Tight design constraints, design goal is usually to minimize the circuit area
  - They NEVER try the circuit without demonstrating a correct simulation after P&R
  - Projects have not been repeated in 20+ years… but ideas have a limit.

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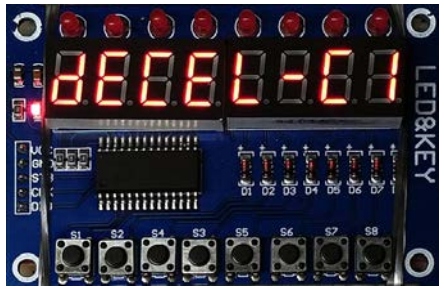
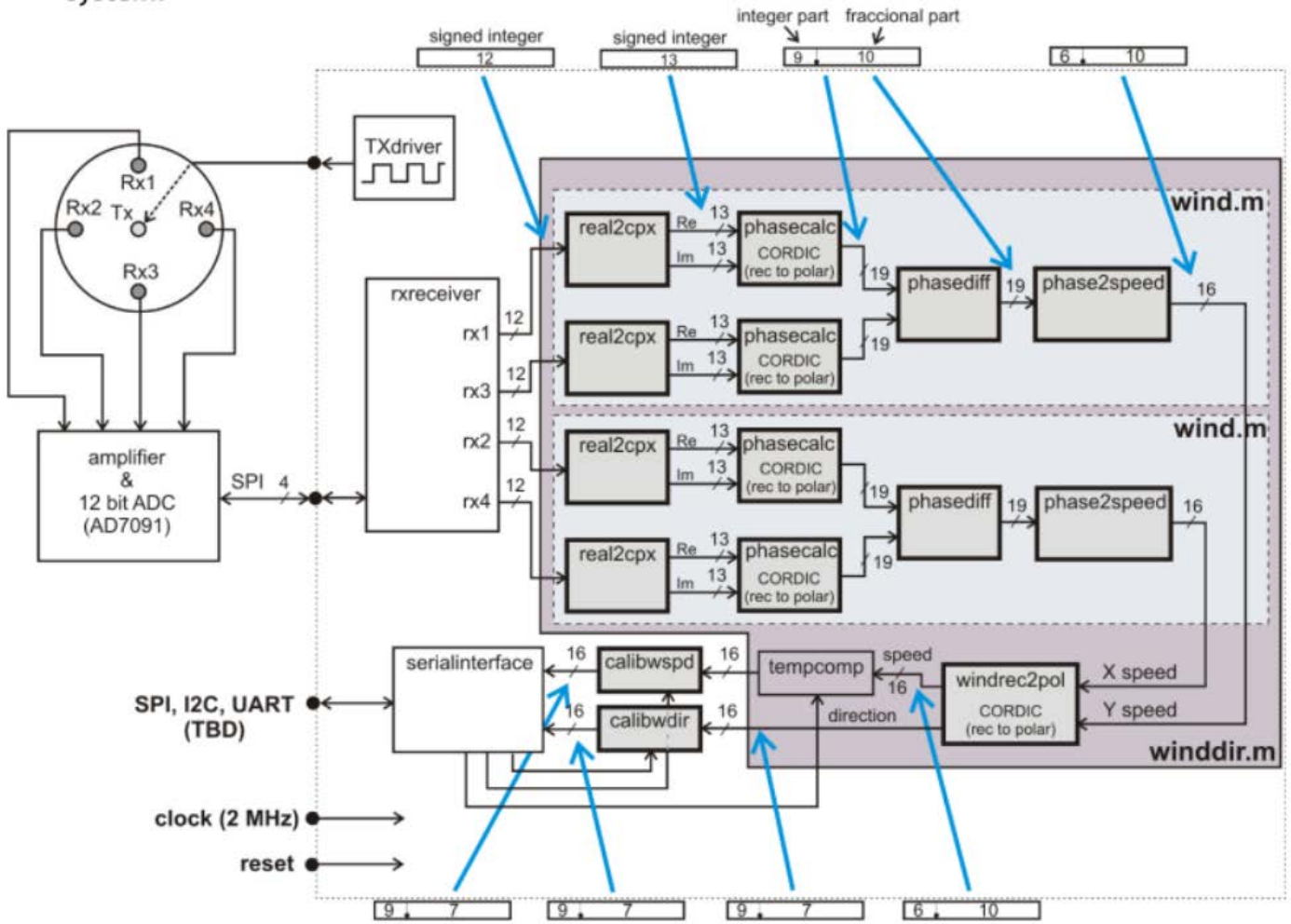
Digital Systems Design
(from HDL models to logic gates)





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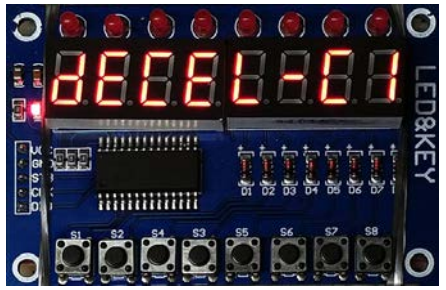
Digital Systems Design
(from HDL models to logic gates)



- Major difficulties
  - Assessment of the lab projects has a high degree of uncertainty
    - Difficult to establish objective metrics
  - Limited resources to allow fully individual works
    - Computers, software licenses, time, teaching staff (~50 students for one teacher)
  - Most of the work is done extra classes, but who does the work ?
    - Main final product is just text (Verilog code), very easy to propagate among the students
    - Too many cases of ideas based on the work of others
  - Significant disparity in the results of the lab works and exams

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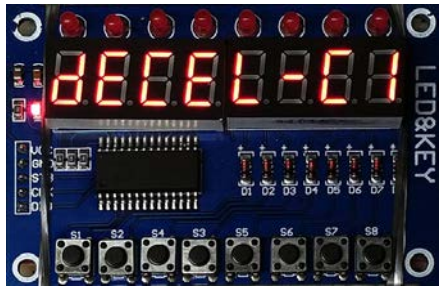
VLSI Circuit Design
(from logic gates to silicon)



- Design flow for custom digital integrated circuits (ASICs)
- Models of the MOS transistor
- Understanding digital integrated technologies
- Modelling of interconnections
- Design and characterization of logic gates at the transistor level
- Transistor sizing and timing optimization
- Full-custom layout design of logic cells
- Parasitic extraction, post-layout simulation (SPICE)

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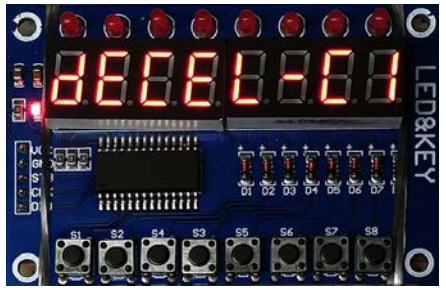
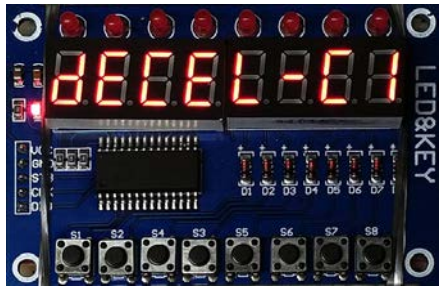
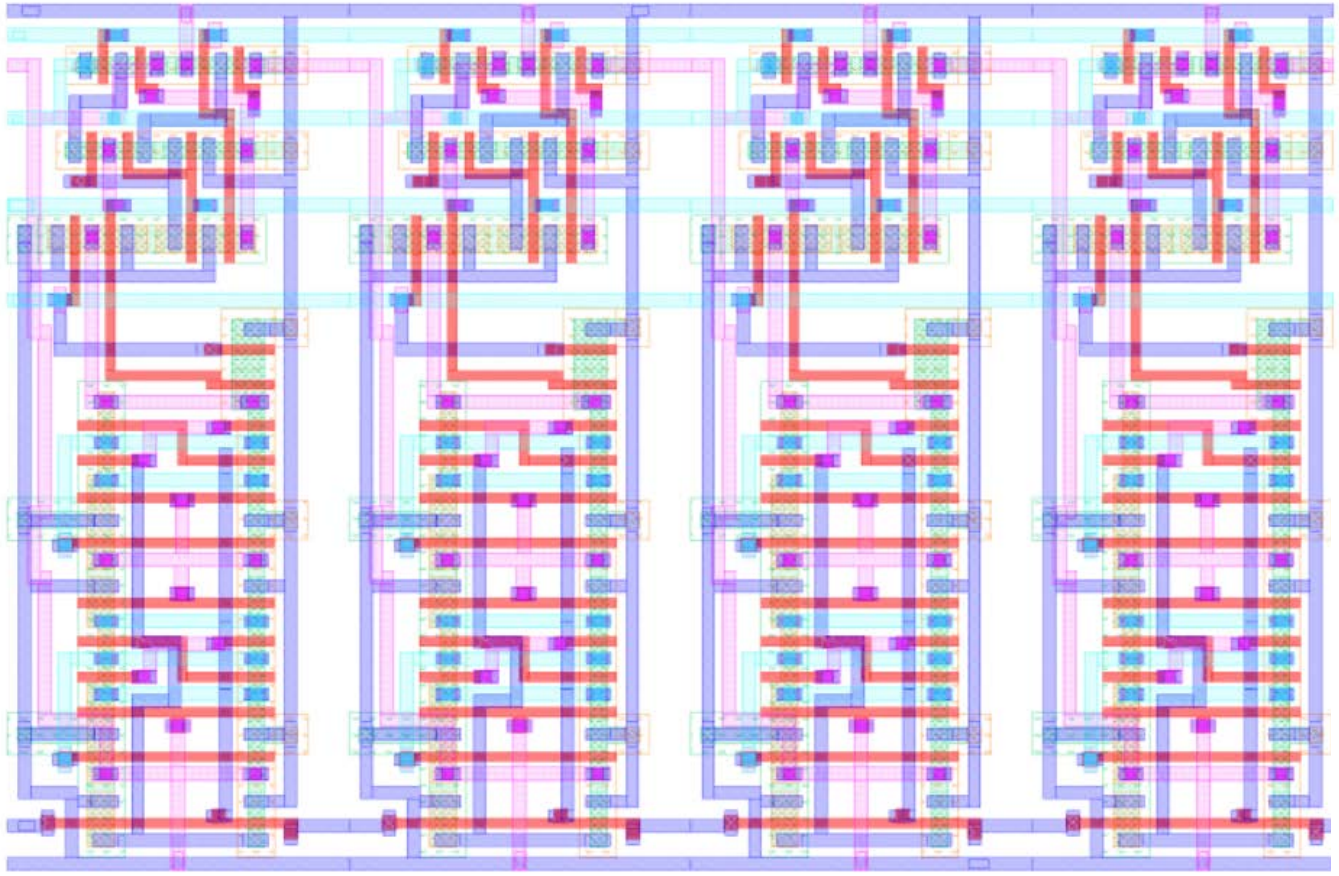
VLSI Circuit Design
(from logic gates to silicon)

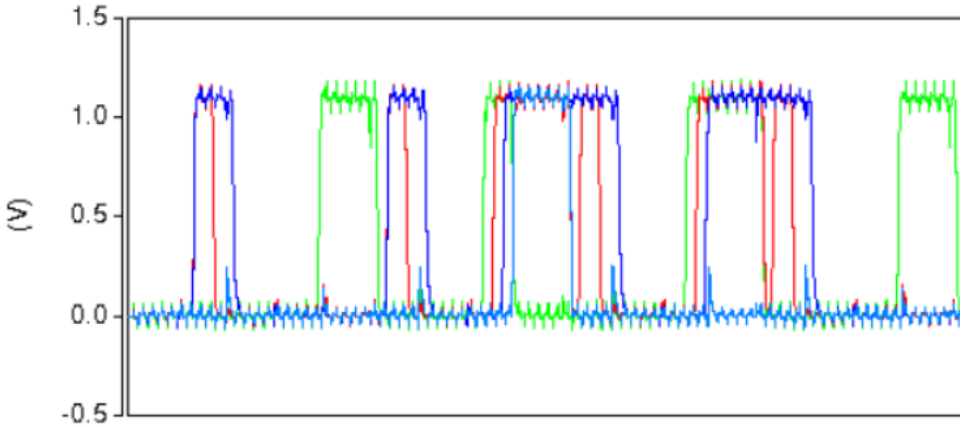


- Organization of classes similar to Digital Systems Design
- More restrictive usage of the industrial EDA tools (Europractice)
  - Cadence tools and HSPICE must be used in that lab, shared with other classes
  - No alternative of free tools
- Final laboratory project is to design and characterize a custom digital cell
  - Constraints and design goals as area, aspect ratio or speed
  - Examples
    - scalable N-bit shift-register, N-bit counter, NXM-bit memory block

VLSI Circuit Design
(from logic gates to silicon)







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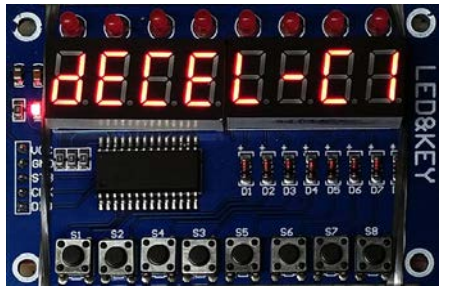
Heterogeneous Systems Architectures
(from software to software + hardware @ embedded systems)



- Performance assessment of software applications
- Code transformations and optimizations
- Interconnections in embedded systems and integrated SoCs
- Design for integrated CPU+FPGA systems (XILINX Zynq7000)
- High-level Synthesis (Vitis HLS) for synthesizing CPU accelerators
- Optimization of interfaces CPU-accelerator-memory

- Digital design is not exercised but must be well understood !

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