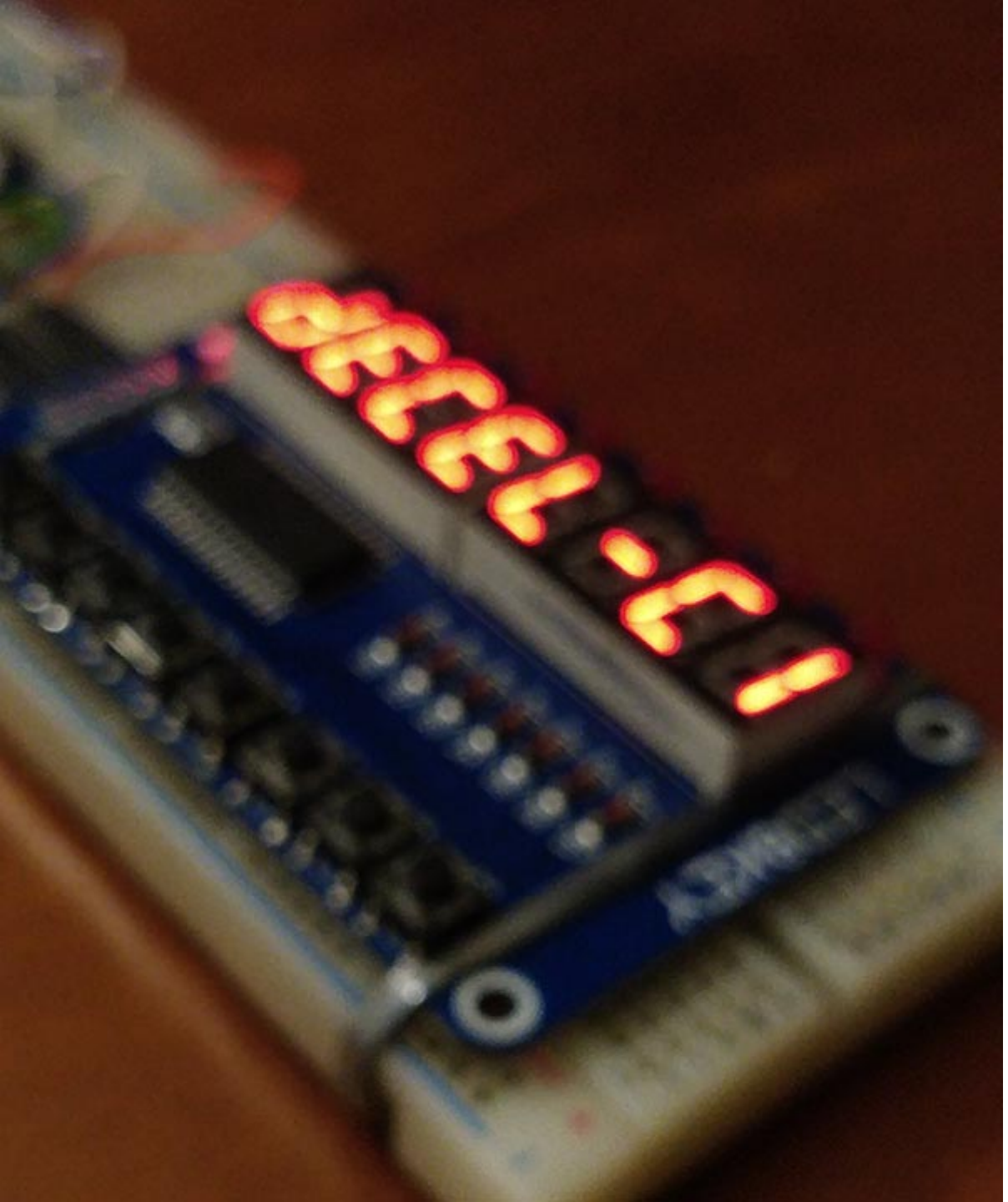


DECEL Project

Training activity C1

Porto, 25-27 January 2023

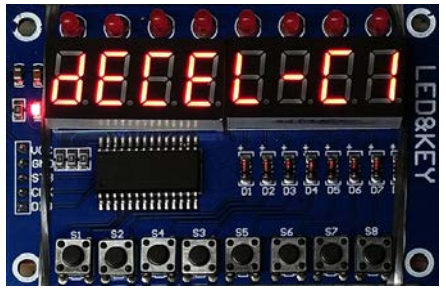
Universidade do Porto

Faculdade de Engenharia

FEUP

Co-funded by
the European Union

Current academic model for engineering in UniFE (B.Sc.)



- 3 years Bachelor course on Electronics and Computer Science
- …first glance of Digital Electronics

1st year

- Mathematics
- Physics
- Programming

2nd year

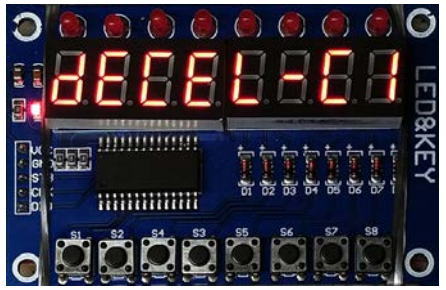
Fundamentals of:
- Computer Science
- Circuits
- Digital Electronics
- Communication
- Automation

3rd year

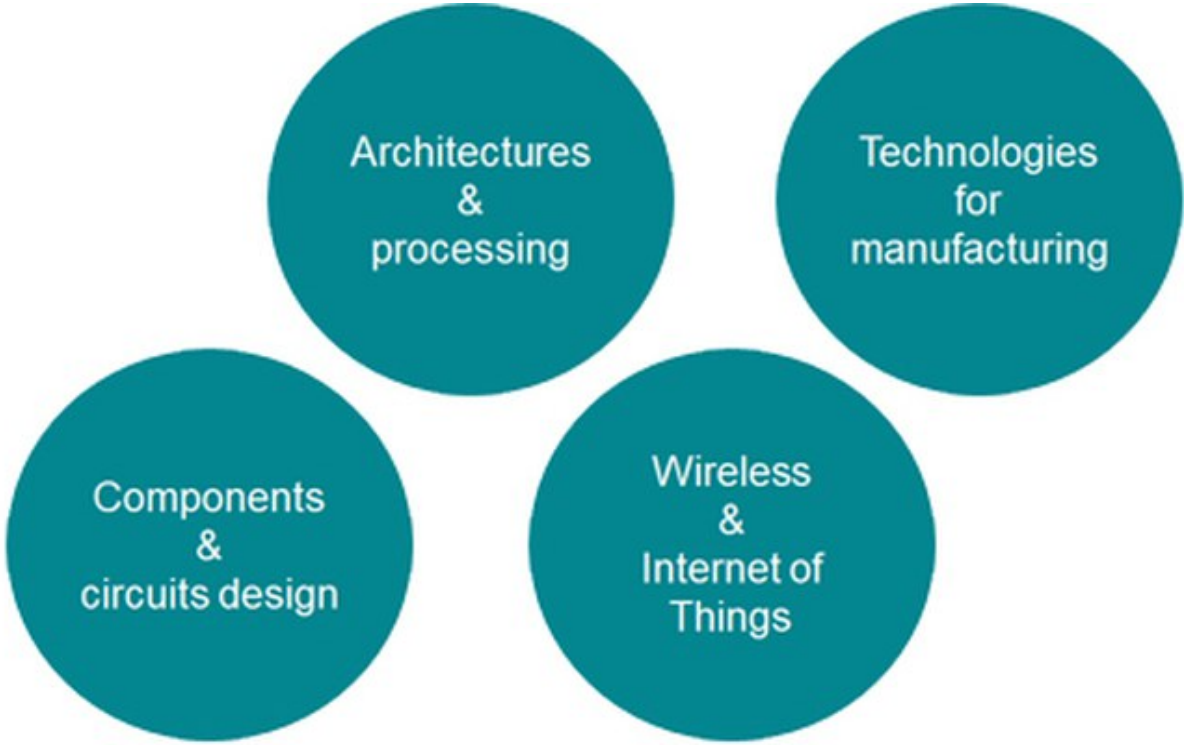
Electronics & Wireless | Web Design | Computer architectures | Robotics

Co-funded by the European Union

Current academic model for engineering in UniFE (M.Sc.)



- 2 years Master course on Electronics for ICT
- 4 specialization branches
- Architectures & Processing
  - Deals with CPU, FPGA and Storage
  - VLSI design with HDL
- Components & Circuits design
  - Analogue/RF-oriented curricula
  - …but with a twist on FPGAs
- Technologies for manufacturing
  - FPGA design for robotics and IA



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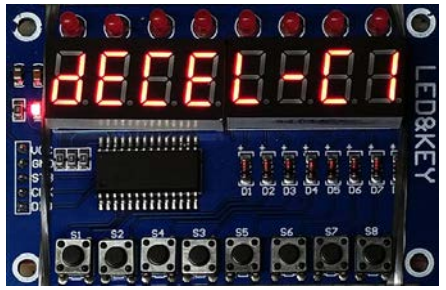
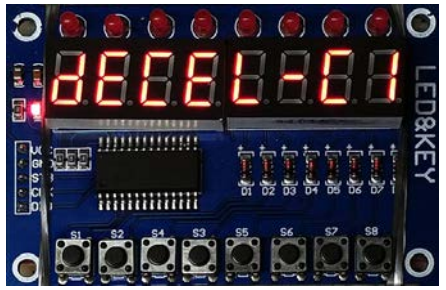
Current academic model for engineering in UniFE (M.Sc.)



- 2 years Master course on Computer Science
- 4 specialization branches
- Industrial automation & Robotics
  - Deals with FPGA design
- Industry 4.0
  - COTS IoT designs
- Other branches are off-scope

Co-funded by the European Union

Digital Electronics Systems Course Syllabus in short



- The course is preparatory to courses dealing with digital systems
  - The 101-class for Electronics in B.Sc.

- Topics addressed: fundamental elements of a digital system
  - Fundamentals of logic gates and of their circuit realization (using CMOS)
  - Evolution of digital circuits
  - Number representation and combinational circuits to realize elementary mathematic operations
  - Fundamentals of sequential circuits, synchronous and asynchronous
  - Fundamentals of information conversion domain (ADC and DAC)
  - A quick glance on storage elements

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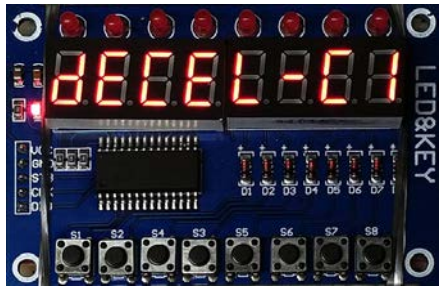
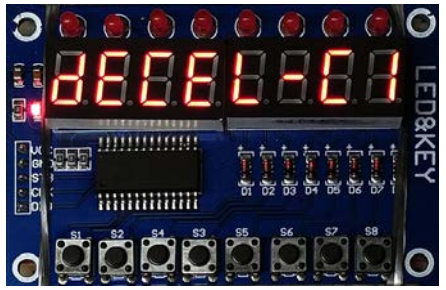
Digital Electronics Systems Course details



Mandatory	YES
Year	2nd
Semester	1st
ECTS	6
Hours	60 (5 hours per week, 12 weeks)
Average number of students	125

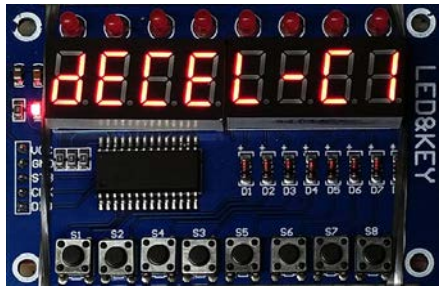
Digital Electronics Systems Teaching methods and Grading



- Teaching methodology
  - Lectures in class on scheduled times
- Teaching material
  - PDF or slide-decks used during lectures
  - During pandemics emergency → Asynchronous video lectures
- Non-traditional teaching activities experimentation
  - Use of an instant poll system (Kahoot!) during any lesson to get a feedback on the degree of understanding of the fundamentals
  - This is the first pilot in Electronics at B.Sc.-level used in class
- Grading process
  - until 2021-2022 a.y. → Moodle test followed by an oral discussion
  - since 2022-2023 a.y. → only Moodle test

Co-funded by the European Union

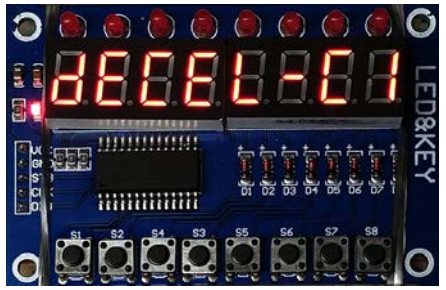
Electronics of Digital Systems Course Syllabus in short



- The course takes up the main topics seen during Digital Electronic Systems (from a logical / system point of view) and examines the circuits in detail
- Topics addressed: analysis and design techniques of VLSI circuits/systems
  - Fundamentals of semiconductor manufacturing technology
  - Fundamental characteristics of a CMOS circuit
  - Basic knowledge to face the study of complex VLSI systems and their interconnections with the constraints imposed by the required performance in terms of cost, speed, area occupation, noise immunity and power consumption
  - Operation and sizing of static and dynamic combinatorial blocks and sequential circuits
  - Timing of electronic circuits with emphasis on distribution of the synchronism signal and deviations from expectations
  - Digital VLSI testing (BIST, JTAG, LFSR, MISR)

Co-funded by the European Union

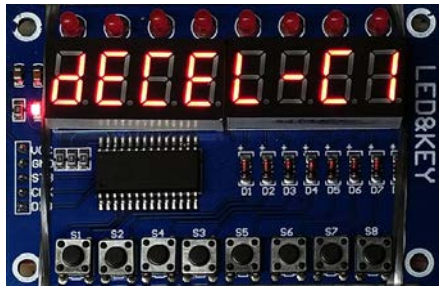
Electronics of Digital Systems Course details



Mandatory	NO*
Year	3rd
Semester	2nd
ECTS	6
Hours	60 (5 hours per week, 12 weeks) Reduced to 30 using flipped class
Average number of students	30

* Mandatory for *Electronics and Wireless* and for *Computer Architecture* branches

Electronics of Digital Systems Teaching methods and Grading



- Teaching methodology
  - Lectures in class on scheduled times
- Teaching material
  - PDF or slide-decks used during lectures
  - During pandemics emergency → Asynchronous video lectures
- Non-traditional teaching activities experimentation
  - Since 2021-2022 a.y. Flipped-Classroom is in place with video recordings of the lessons available before the lecture. In class there is a fundamental points discussion about different VLSI design choices and exercises solving
  - In 2022-2023 a.y. an instant poll system (Kahoot!) will be used
- Grading process
  - Moodle test followed by an oral discussion

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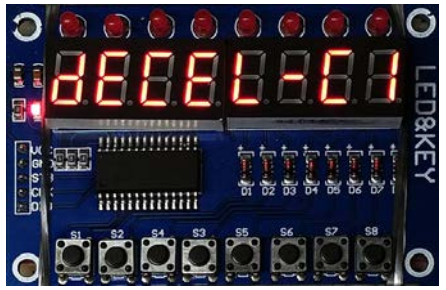
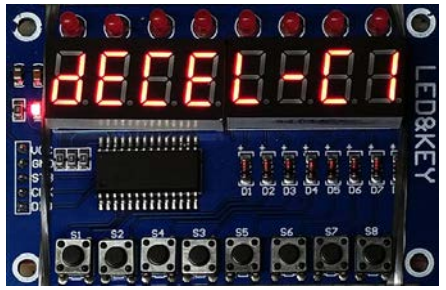
Hardware Description Languages Course Syllabus in short



- Introduction to Hardware Description Languages and their role in logic design for students interested in computer architecture
- Topics addressed: logic synthesis and HDL constructs
  - VHDL language fundamentals
  - Syntax and semantic
  - Event driven simulation
  - High-level synthesis from behavioral models to Extended Finite State Machines
  - Scheduling and allocation fundamentals and algorithms

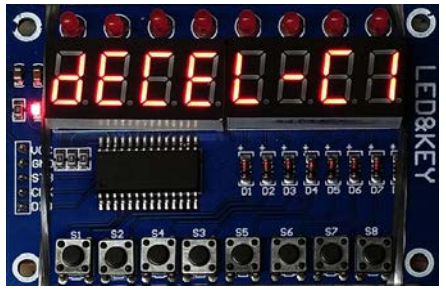
Hardware Description Languages Course details



Mandatory	NO*
Year	3rd
Semester	1st
ECTS	6
Hours	60 (5 hours per week, 12 weeks)
Average number of students	30

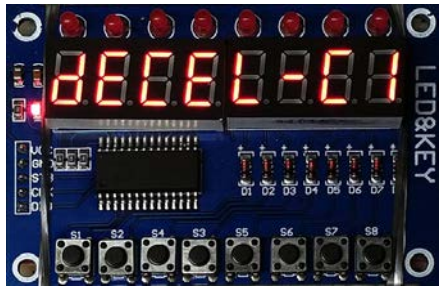
* Mandatory for *Computer Architecture* branch

Hardware Description Languages Teaching methods and Grading



- Teaching methodology
  - Lectures in class on scheduled times
  - Laboratory activities concerning the building and simulation of VHDL models exploring the language modeling capabilities at different abstraction levels
- Teaching material
  - PDF or slide-decks used during lectures
  - During pandemics emergency → Asynchronous video lectures
- Tools for laboratory
    - Use of ALDEC/Modelsim simulators and tool available in EDAplayground platform
- Grading process
  - Written examination + a project to be developed after the end of the course

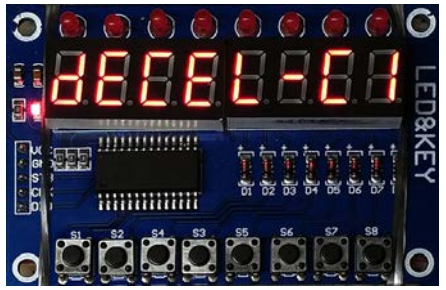
Design automation for Dig. systems Course Syllabus in short



- The course aims to provide understanding of data-structures, algorithms and tools used in logic level synthesis, testing and verification for computer scientists
- Topic addressed: General tools for model and design verification
  - Boolean Networks, BDDs, AIGs, Boolean Satisfiability
  - Logic synthesis and optimization
  - Combinational and sequential circuits
  - Testing and fault modeling with simulation
  - Test generation
  - Design verification and combinational verification via SAT
  - Model checking

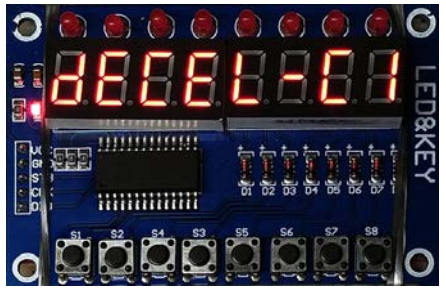
Co-funded by the European Union

Design automation for Dig. systems
Course details



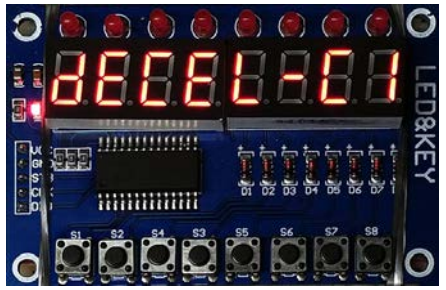
Mandatory	NO
Year	Alternate (odd years) for Computer Science M.Sc.
Semester	2nd
ECTS	6
Hours	60 (5 hours per week, 12 weeks)
Average number of students	15

Design automation for Dig. systems Teaching methods and Grading



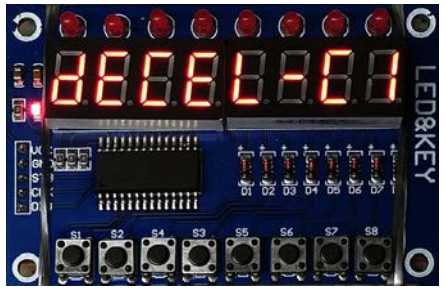
- Teaching methodology
  - Lectures in class on scheduled times
  - Laboratory activities regard the use of open-source tools implementing the algorithms presented during the lectures
- Teaching material
  - PDF or slide-decks used during lectures
  - During pandemics emergency → Asynchronous video lectures
- Tools for laboratory
    - Use of ALDEC/Modelsim simulators and tool available in EDAplayground platform
- Grading process
  - Oral examination + a software project to be developed after the end of the course consisting in the implementation of a simplified version of the presented algoritmhs

FPGA Laboratory Course Syllabus in short



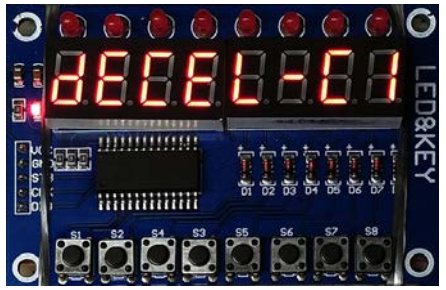
- The course provides the necessary elements for prototyping and design of integrated electronic systems using FPGA devices
- Topic addressed: Design of a digital reconfigurable system
  - Fundamental elements of an FPGA
  - Knowledge of a hardware description language (VHDL) oriented to the simulation and implementation of an electronic system
  - Knowledge of an integrated development environment (Xilinx Vivado) for FPGA
  - Knowledge related to the constraints of area occupation, memory, and power consumption of an electronic system implemented on FPGA
  - Communication protocols like SPI and I2C for external devices such as off-chip memories, human interface devices, ADCs, accelerometers, and displays
  - Interfacing an analog electronic signal with a digital electronic system to build and process a signal using the mixed-signal paradigm

FPGA Laboratory Course details



Mandatory	NO
Year	Alternate (even years) for Electronics for ICT M.Sc.
Semester	2nd
ECTS	6
Hours	60 (5 hours per week, 12 weeks)
Average number of students	25

FPGA Laboratory
Teaching methods and Grading



- Teaching methodology
  - Mainly laboratory activities regard the use of Xilinx Vivado platform for FPGA design
  - 3 Lectures in class on scheduled times only for VHDL fundamentals
- Teaching material
  - PDF, slide-decks, and data sheets used during lectures and laboratory activities
  - During pandemics emergency → Asynchronous and synchronous video lectures
- Tools for laboratory
    - Digilent Basys3 board, Lab. Benches with oscilloscope and function generators
- Grading process
  - Examination through the development of an assigned Xilinx Vivado project to be carried out within a limited time (3 hours) set by the teacher

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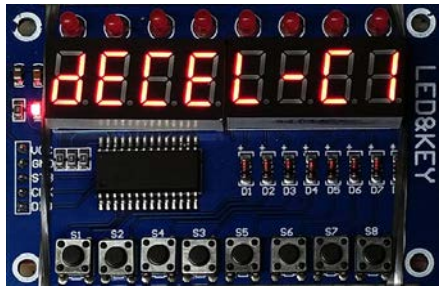
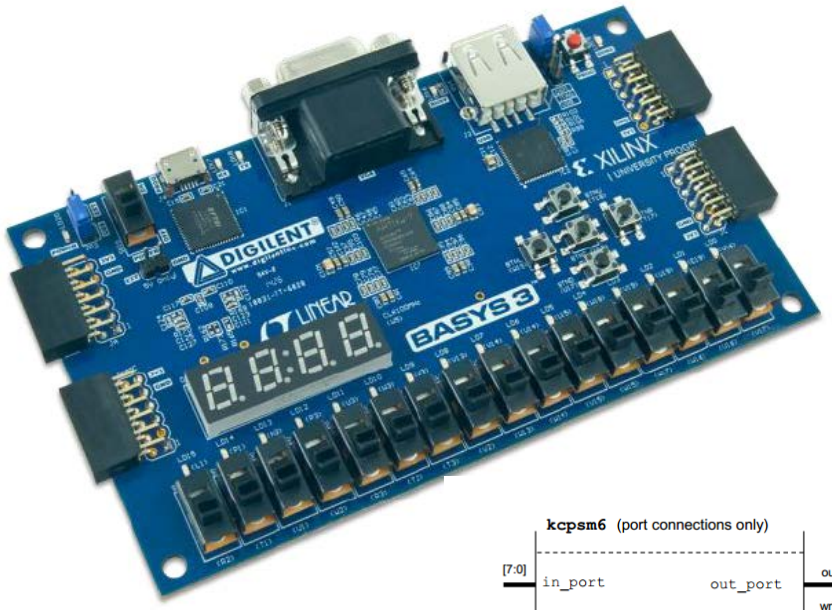
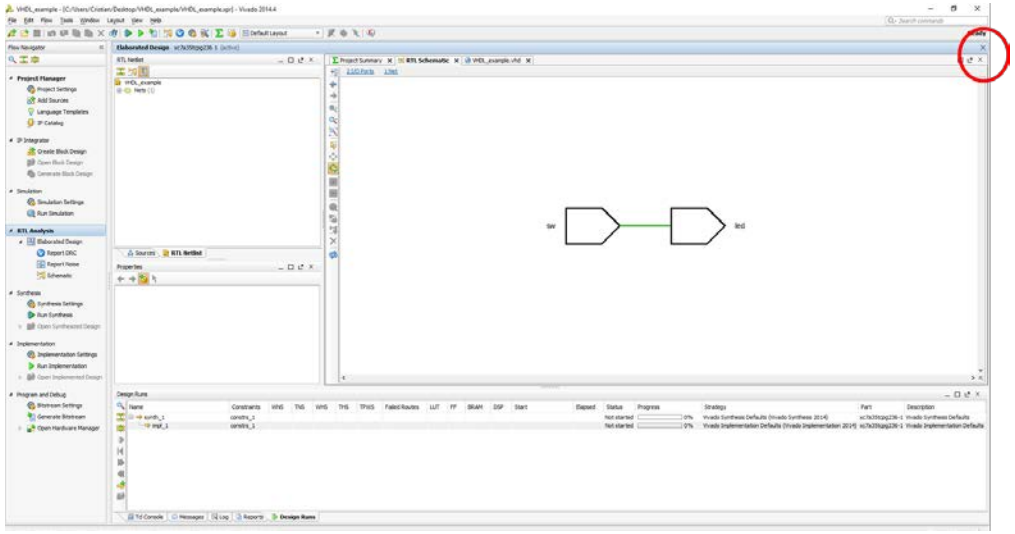
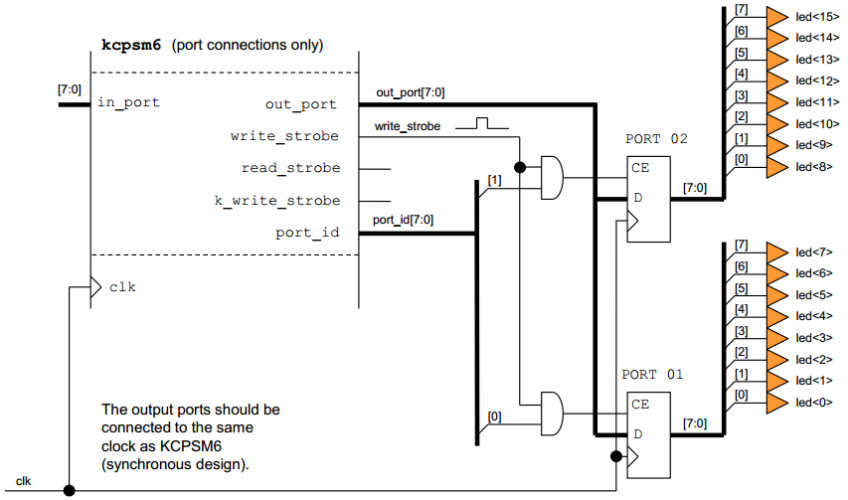
Some tools at work...









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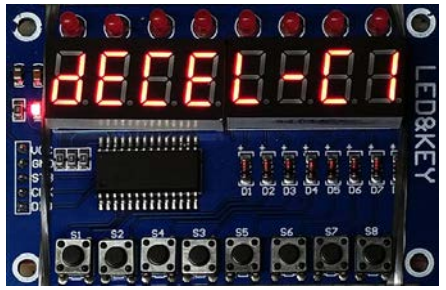

Thanks for your kind attention!

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